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Voltage Balancing Control in Three Level Diode Clamped Inverter Using Carrier Based Offset Addition

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Abstract: Three-level Neutral-Point Clamped (NPC) inverter has become established to be a preferred topology for medium-power motor drive applications operating at several kilovolts. Still several research continues to find solutions to the problem of maintaining a stable neutral-point voltage in the converter. This paper presents the analysis and simulation of a three-level diode-clamped multilevel inverter, employing a sine-triangle modulator with addition of continuous variable offset voltage which regulates the midpoint potential of the dc bus. By maintaining dc-bus voltage balance, a significant reduction in the voltage distortion at the neutral point and also allowing a definitive reduction in the required dc bus capacitance. The effectiveness of the Pulse Width Modulation (PWM) strategies developed with continuous offset addition is demonstrated by MATLAB/SIMULINK based simulation presented in this paper.

Keywords*:* NPC inverter; 3 phase induction motor; offset addition; carrier based PWM; dq theory; pi control

I. INTRODUCTION

Diode clamped/Neutral point clamped multilevel inverter technology has emerged recently as a very important alternative in the area of high-power medium voltage energy control. The structure of diode clamped inverters allows them to reach high voltages and therefore lower voltage rating devices can be used. As the number of levels increases the synthesized output waveform has more steps producing a very fine stair case wave and approaching very closely to the desired sinusoidal wave.

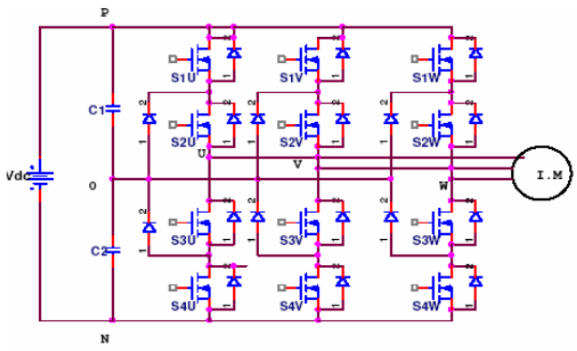

Fig.1. Three phase three-level NPC

Hence diode clamped multilevel inverters offer a better choice at a high power end because the high volt-ampere ratings are possible with these inverters without the problems of high dv/dt and the other associated ones.

NPC inverter has an inherent problem of unbalanced voltages across dc-link capacitors due to load unbalancing, non uniform distribution of charges, and non-identical properties of dc-link capacitors provided from the manufacturer [1], [2]. Several open loop strategies have been proposed for the reduction of the harmonic content [3], [4].

The authors have proposed two ways of mid-point voltage balancing in NPC three level inverters. One way of voltage balancing based upon the addition or modification of hardware circuitry to the inverter [5]-[10] which modify the charging and discharging currents of DC-link capacitors.

Second way of voltage balancing is based upon modification in inverter control strategy based on PWM schemes. Many carrier and SVPWM based strategies have been proposed for the modulation of theses inverters [11]-[15].

Table 1: Switching states of three level NPC inverter

S1U	S2U	S3U	S4U	Switching states	Voltage output(Vuo)
1	1	0	0	+	+Vdc/2
0	1	1	0	0	0
0	0	1	1	-	-Vdc/2

A closed loop control strategy, which reduces the harmonic content as well as maintains voltage stability in the neutral point is presented in this paper. Closed loop regulator is based on injecting offset magnitude to the modulating signal as a function of a control input that corrects any existing imbalance.

In this paper main considerations given to regulate the voltage imbalance of NPC inverter employing sine-triangle modulator in conjunction with a closed-loop controller, which considerably reduces the harmonic distortions in the output voltage waveform, resulting in reduction of the required dc bus capacitance.

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II. NEED OF NEUTRAL POINT BALANCING

The Neutral point clamped inverter is showed in Fig.1 and Table I give the switching states to generate the three level output voltage for phase U.

Due to unequal voltages across two dc-link capacitors PWM inverter output voltage and output current waveforms get distorted. Unbalance DC link creates increased voltage stress on switching devices. Increased voltage imbalance across dc-link capacitors may cause failure of devices. Therefore, Neutral point voltage balancing control is necessary without sacrificing the harmonic performance of the inverter. Fig. 2(a) and (b) shows the waveforms and harmonic spectrums of phase voltage and line voltage under burst condition of large imbalance at dc link with *V*dc1 = 200 V and *V*dc2 = 400 V. Under this condition, the dc component and even-order harmonics are more significant which are dangerous for drive and other applications.

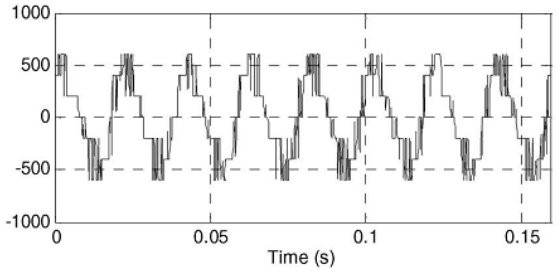

Fig. 2 Output line voltage distortions due to unbalanced DC-link voltage

Table II gives the effect of dc-link imbalance on % THD with a total dc-link voltage of 400 V. For this study, the dc link was intentionally made unbalanced. It is clear that the line voltage THD will have the minimum value for balanced dc link and they are increasing with increased unbalancing

Table II: Effect of DC link imbalance on output %THD (Vdc=600V).

Vdc1	Vdc2	Fundamental Line voltage	%THD line voltage
230	370	469	25.4
240	360	471	21
250	350	492	19.7
300	300	494	16
350	250	485	16.5
400	200	489	25
450	150	495	32.7

III. DESIGN OF CLOSED LOOP NPC INVERTER

Designing of closed loop NPC inverter consider the following important aspects,
i) ensuring dc-link capacitor, voltage balancing and regulating dc-link voltage
ii) minimization of inverter voltage and current harmonics; iii) ensuring less and uniform switching stress on switching devices, resulting in reduced switching losses.

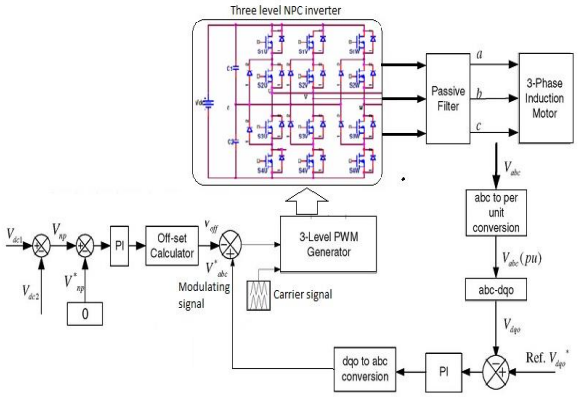

Fig.3 NPC offset addition PWM block diagram

Fig. 3 shows the complete block diagram of the NPC offset addition PWM. It consists of both a dc-link voltage control loop and a load voltage control loop. Three phase load voltages are sensed and converted into *dqo*-axis. After comparing with preset values (Vd=1,Vq=0) again converted to abc-signal. This Vabc signal is added with the dc-link voltage control loop generated offset signal. This signal is acting as modulating signal. It is compared with carrier PWM by using level shift PWM and the pulses are given to appropriate switches.

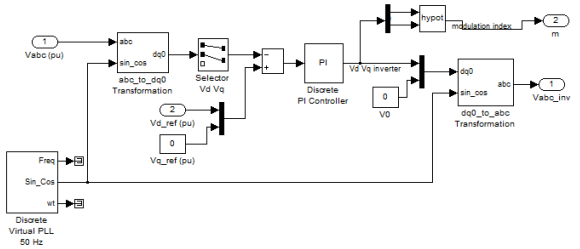

Fig.4 abc to dqo conversion reference comparison and dqo to abc conversion

Fig shows the measured voltage Vabc is converted by using the abc to dqo converstion method using the following three-phase to two-phase conversion:

$Vd = 2/3[Va \sin(\omega t)+Vb \sin(\omega t - 120^o)+Vc\sin(\omega t - 240^o)]$
$Vq = 2/3[Va \cos(\omega t)+Vb \cos(\omega t - 120^o)+Vc \cos(\omega t - 240^o)]$
$Vo = Va+ Vb +Vc$

These *dqo* voltages *Vdqo* are compared with preset values of *dqo* voltages. It results in voltage error which is processed through a PI controller to generate two axis command signals *V*dqo*. Then, three-phase reference voltage signals are synthesized using the following two-phase to three-phase conversion:
$V_a = V_d \sin(\omega t) + V_q \cos(\omega t) + V_o)$
$V_b = V_d \sin(\omega t - 1200) + V_q \cos(\omega t - 1200) + V_o)$
$V_c = V_d \sin(\omega t - 2400) + V_q \cos(\omega t - 2400) + V_o)$
These are the reference sinusoidal modulating signal V_{abc^*}. The amplitude modulation index *m* is defined as

$$m = \sqrt{V_d^2 + V_q^2}$$

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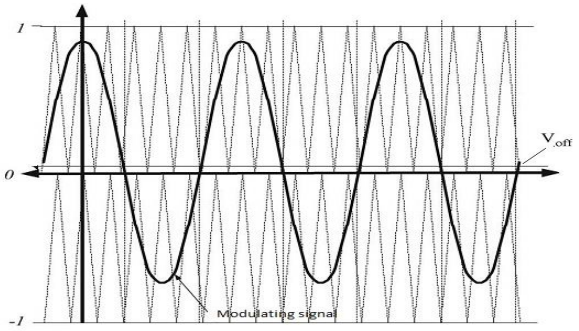

Fig.5 Offset addition PWM

offset addition method is shown in Fig. to the reference sinusoidal signal. The compared signal is given to switches as sequence in the corresponding legs.

IV. SIMULATION RESULTS

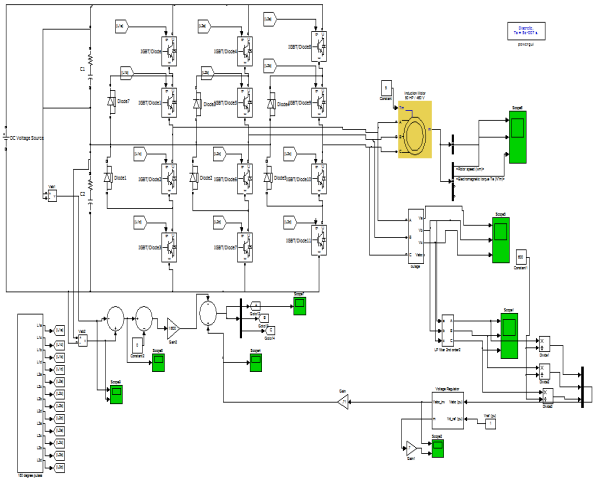

Fig.6 A MATLAB/Simulink model of three-phase three-level DCMLI with the carrier-based offset addition PWM

MATLAB/Simulink model of three-phase three-level DCMLI
with the carrier-based offset addition PWM is shown in fig.6

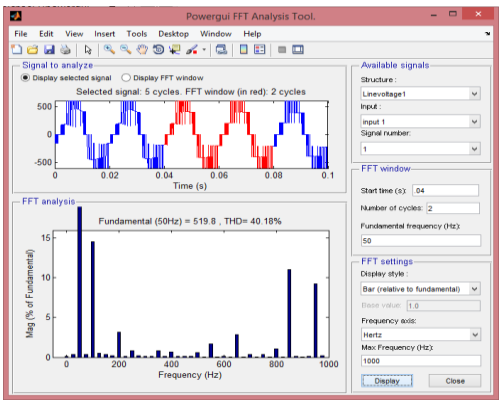

Fig.7 Simulated inverter line voltage (Vab) and its frequency spectrum with unbalanced dc link without closed loop offset PWM and

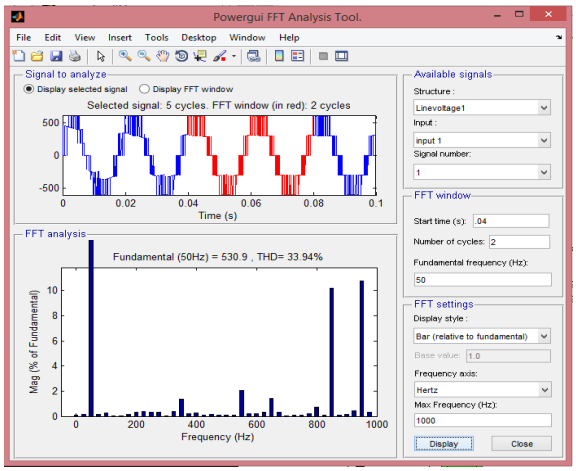

Fig.8 Simulated inverter line voltage (Vab) and its frequency spectrum with unbalanced dc link with Neutral point balancing.

Frequency spectrum of output line voltage without closed loop offset PWM are shown in Fig. 7 with fundamental value as 519.8 and 40.18 % of THD. In Fig.8 frequency spectrum for closed loop NPC inverter with offset addition PWM is shown with fundamenatal value as 530.9 V and THD values as 33.94%

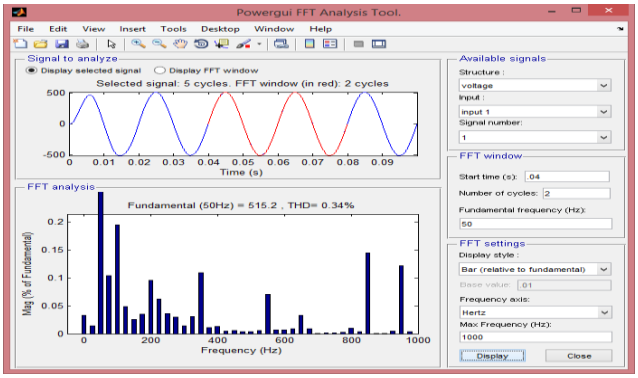

Fig.9 Simulated inverter line voltage (Vab) and its frequency spectrum with unbalanced dc link with neutral point balancing after filtering.

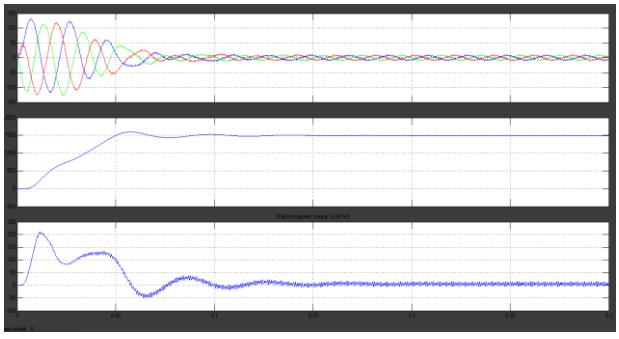

Fig.10 Stator current waveform (Ia, Ib and Ic) , Motor speed (rpm), Electromagnetic torque waveforms under balanced dc link voltages after neutral point voltge balancing.

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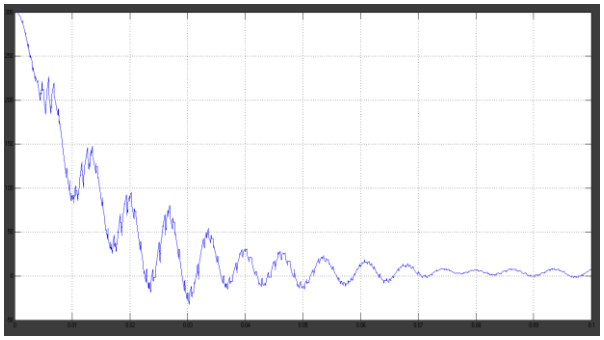

Fig.11 Neutral point voltage (Vnp= Vdc1-Vdc2)

V. CONCLUSION

A simple carrier-based neutral voltage balancing for a three-level diodeclamped inverter in conjunction with a closed-loop controller has been proposed in this paper. The proposed offset calculation PWM gives improved inverter performance in terms of reduced THD,with unbalanced dc-link voltages,improved NPP harmonic profile, and balanced dc link with almost zero average Neutral point potential. The novelty of the proposed mehtod is in the determination of the magnitude of variable offset voltagebasedupon the average value, peak-to-peak amplitude,THDs,and third harmonic content in NPP.This not only regulates the NPP but also reduces the harmonic contents in inverter output voltages and currents. Simultaneously, second-order harmonics in inverter output voltage get eliminated which may otherwise produce torque pulsations, harmonic currents, and additional power losses. Aside from maintaining the dc-bus voltage balance, the proposed closed loop offeset voltage PWM leads to a significant reduction in the voltage distortion.

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